CHARACTERIZATION OF THERMAL EFFECTS ON MICROWAVE TRANSISTOR PERFORMANCE USING AN EFFICIENT PHYSICAL MODEL

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ABSTRACT

A physical model is described which is capable of predicting the effects of self-heating on MESFET performance whilst being efficient enough to run on a personal computer. Comparisons with the true DC characteristics for a number of devices of different gate lengths and microwave measurements demonstrates the validity of the model.

INTRODUCTION

Power dissipation in microwave transistors can lead to a significant reduction in performance and reliability. Under certain bias conditions MESFETs can have 'hot spots' in the region between the gate and the drain in excess of 100°C above ambient temperature.

The inclusion of the effects of temperature in equivalent circuit models is problematic as well as requiring accurate device characterization. Recent work on the effects of temperature have produced quite different relationships for the equivalent circuit model element values as a function of temperature [1,2]. The use of equivalent circuit models also makes the separation of the effects of self-heating and ambient temperature difficult to establish.

Attempts have been made to include self-heating in physical models [3,4]. These two-dimensional electro-thermal models have been shown to be in very close agreement with measured device characteristics but are unsuitable for CAD due to their extremely large computational requirements. This paper describes an efficient physical MESFET model capable of predicting the effect of self-heating on both DC and microwave performance, which is well suited to process-orientated CAD.

MODEL DESCRIPTION

The physical model used in this work has been developed from the quasi-two-dimensional MESFET model developed by Snowden and Pantoja [5] at the University of Leeds. It is based on the solution of Poisson's Equation and the Boltzmann Transport Equation for a MESFET. The field in the channel is assumed to be mainly one-dimensional whilst a two-dimensional description of the channel is retained. As a result quasi-two-dimensional models are approximately three orders of magnitude faster than full two-dimensional models whilst retaining a good degree of their accuracy. A thermal model has been included improving the accuracy and applicability of the model.

Figure 1 shows the temperature distribution in a MESFET produced by a two-dimensional electro-thermal model [4]. The temperature distribution is far from uniform but the variation of temperature close to the gate depletion region, which is the critical part of the active channel governing device performance, is relatively small. Assuming a constant temperature distribution in the channel, the channel temperature can be approximated using the expression

$$T_{chan} = I_{ds} V_{ds} R_{th} + T_o \qquad (1)$$

where T_{chan} is the active layer temperature, T_o is the ambient temperature and R_{th} is the thermal resistance, which can be measured or estimated from a closed-form relationship [6]. The low field mobility, μ_o, is a strong function of temperature and is described using the expression developed by Blakemore [7]

$$\mu_o (T_{chan}) = \mu_o (T_o) \left(\frac{T_o}{T_{chan}} \right)^{2.3} \qquad (2)$$

The gate barrier height, V_{bi}, is a function of temperature and can be described by the following expression

$$V_{bi} (T_{chan}) = V_{bi} (T_o) - k_T (T_{chan} - T_o) \qquad (3)$$

where k_T has a value between 1.6 and 0.26mVK^{-1} [8,9]. The relative permittivity, ϵ_r, is also temperature dependent and a relationship of the following form is used

$$\epsilon_r (T_{chan}) = \epsilon_r (T_o)(1 + B_\epsilon (T_{chan} - T_o)) \qquad (4)$$

The constant B_ϵ has a value of between 0.9 and 1.2x10^{-4}K^{-1} [2,7]. The change in permittivity and barrier height slightly

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alter the gate depletion depth and hence the gate capacitance. At each point in the channel the mobility and steady state electric field are found as a function of electron energy and lattice temperature using curve fits in a similar manner to Carnez et al [10].

The original quasi-two-dimensional model was current driven in that I_{DS} and V_{GS} were specified at each bias point, and V_{DS} was calculated. Due to the coupling between current flow and thermal effects, and the reduction in I_{DS} at high gate and source bias levels an iterative method is required for modelling thermal dependence. For a DC simulation, values of V_{GS}, I_{DS} and V_{DS} are specified. The channel temperature is calculated and this value then used in the previously described relationships. The value of current is modified iteratively until a consistent value is found for the two specified voltages. Typically 100 DC points can be calculated on a 33MHz 486 personal computer in less than two minutes.

In the case of small-signal microwave simulation, the period of the signal is far smaller than the thermal time constants of the device and so the temperature distribution within the device is dependent on the constant DC bias. S-parameter simulation over 1-25GHz at one bias level is performed in less than twenty seconds on a similar personal computer using our physical model.

RESULTS

The model was used to simulate a GEC-Marconi half-micron recessed gate device fabricated from ion-implanted material. The thermal resistance of the device was measured at 75KW^{-1}. Figure 2 shows a comparison between measured and simulated I-V characteristics (with and without the inclusion of thermal effects). Excellent agreement between the measured and simulated results was obtained, especially for the output conductance at high power levels. It should also be noted that no fitting of parameters was required to produce this agreement, and all the physical data required for the model was readily available from the process information.

Figure 3 shows a comparison of measured and simulated DC characteristics for two recessed gate devices fabricated from MOCVD grown material. The devices are single finger T-gate devices with a 200μm gate width. Device (a) had a gate length of approximately 1.5μm whilst device (b) had a gate length of around 1.1μm. The thermal resistance was estimated using the relationships in [11] with twice the gate length being used for the equivalent thermal heat source width. As can be seen the agreement is again very good. Here only the recess depth of the device has been adjusted to give good agreement near pinch-off (due to the absence of accurate geometrical data in the range of the recess depths). Better agreement could have been obtained at high gate and drain bias with the choice of a slightly wider heat source but this was not the point of the exercise. Figure 4 shows a comparison between the DC characteristics of six

devices randomly chosen from a 10mm square section of the wafer, with simulated characteristics obtained using nominal device data. Again good agreement is obtained and it should be noted that nominally identical devices dissipating similar power show slightly different output conductances which negates any benefit of closely fitting results to a single device characteristics.

The model can also be used to predict the change in equivalent circuit element values as a function of temperature whether this is due to self-heating or due to the ambient temperature. Anholt [2] recently suggested that the element values have a linear change with temperature whilst Laskar [1] found non-linear curve fits gave the best agreement with experimental results. Figure 5 shows the gate-source and gate-drain capacitance as a function of temperature and drain-source voltage, with V_{GS} set to +0.4V. Anholt [2] showed a similar relationship for experimental data. The change in capacitance with temperature is due to the reduced depletion depth with the decrease in barrier height. Figure 5 also shows a significant change in C_{gd} with temperature.

The validation of the model under small-signal conditions was carried out using a pulsed S-parameter measurement system. The main source of power dissipation in the device is the DC bias and so with a constant gate bias and a pulsed drain bias the evolution of S-parameters with time and hence temperature can be studied. Measurements were made after 400ns and 2ms of a drain pulse allowing for the device to heat up and for the trap occupancy to reach approximate steady state [12]. The main effect of this pulsed measurement is a reduction in the magnitude and a slight decrease in the phase of S_{21}. The other S parameters remain largely unchanged. This can be explained by the reduction in transconductance due to the reduced electron velocity under the gate with the rise in active layer temperature. Figure 6 shows the comparison between measured and simulated S_{21}. During the pulse the drain current fell from 75.1 to 67.6mA and it is this bias current that is used in the active region temperature calculation. The drain voltage was set to 5.0V and gate voltage was set to 0.0V. It can be seen that above cut-off frequency, the model predicts the change in S_{21} quite well. A better fit could be obtained by optimizing the device parasitics if necessary.

CONCLUSION

This paper has outlined an efficient physical model capable of predicting the effects of self-heating as well as ambient temperature on the DC and microwave characteristics of MESFETs. Excellent agreement has been obtained with measured characteristics for a range of gate length devices for both DC and microwave characteristics. The model provides great insight into device behaviour and is capable of relating physical structure to device performance whilst still being efficient enough to run on a personal computer.

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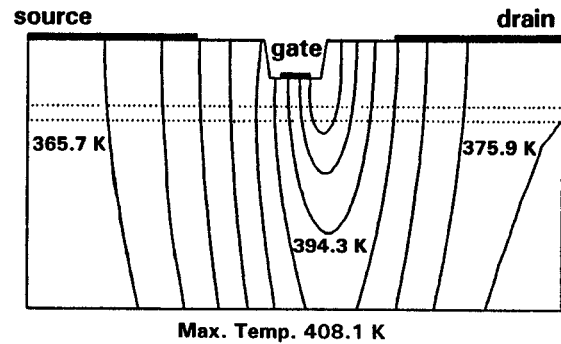
Max. Temp. 408.1 K

Figure 1 *Temperature Distribution in a MESFET produced by a Two-Dimensional Simulation [4]*
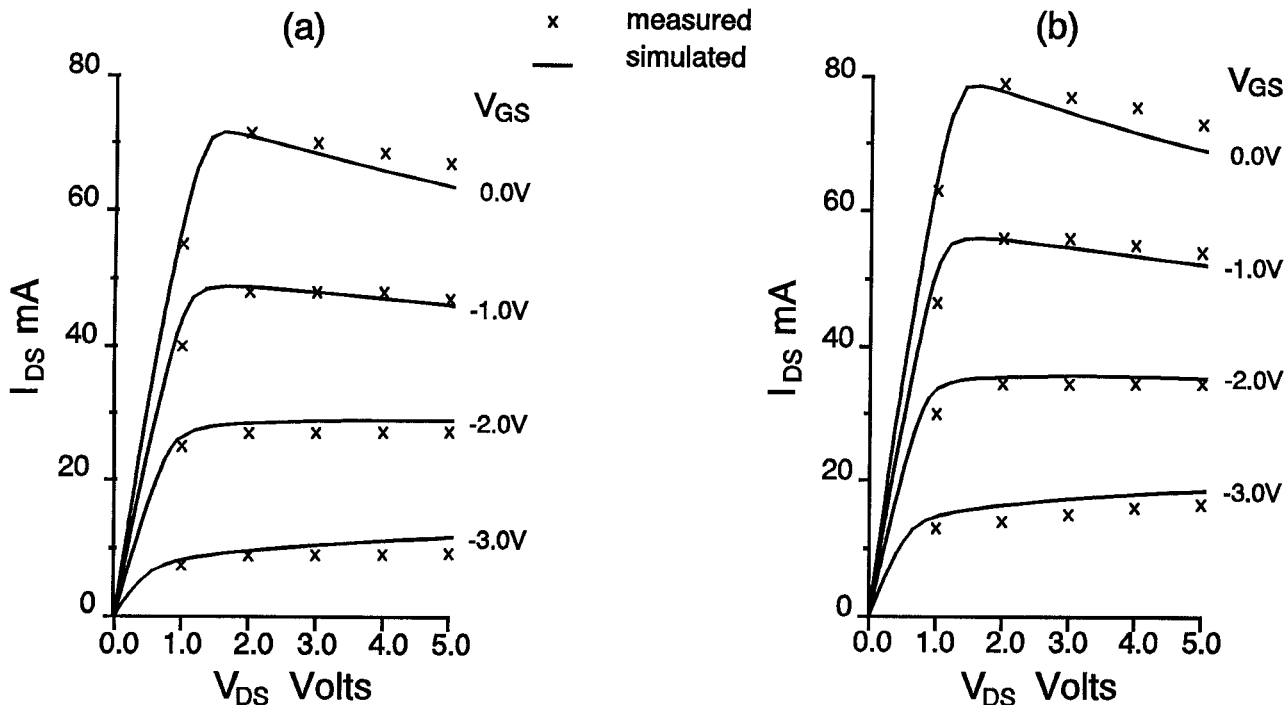

Figure 3 *Comparison Between Measured and Simulated DC Characteristics for (a) 1.5μm and (b) 1.1μm Gate Length Devices*
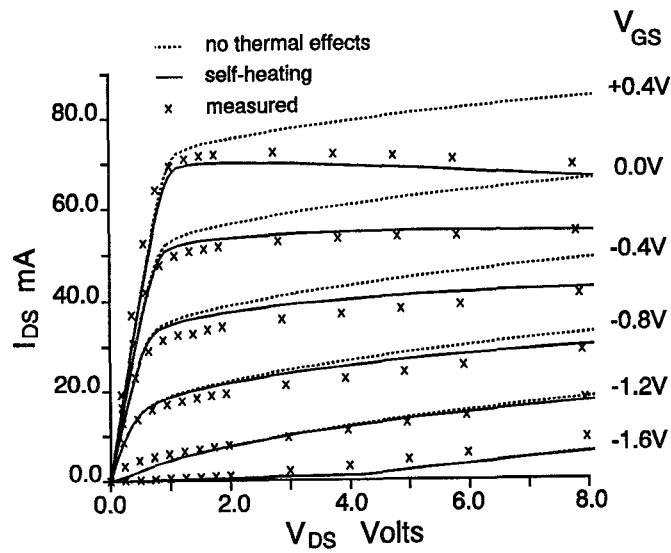
Figure 2   *Comparison Between Measured and Simulated DC Characteristics for a Half-Micron GEC-Marconi MESFET*
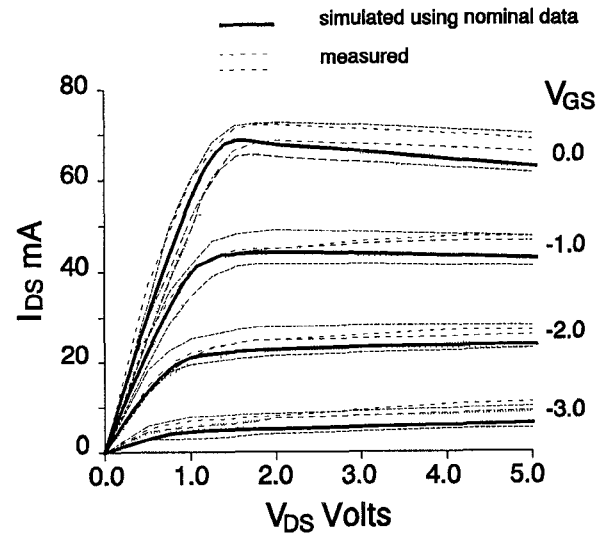
Figure 4   *Comparison Between Measured and Simulated DC Characteristics Obtained Using Nominal Device Data*
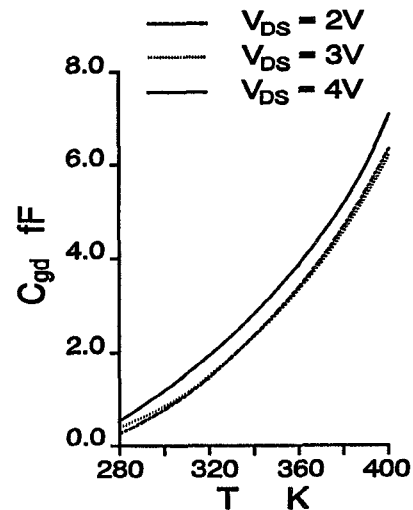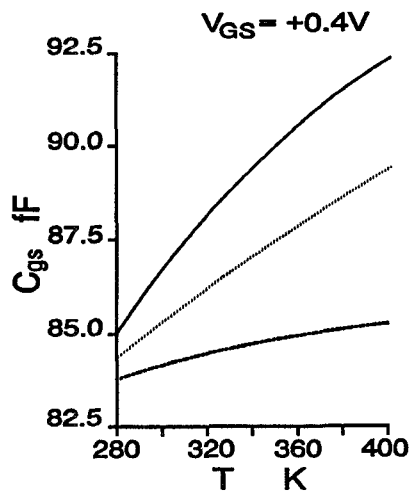
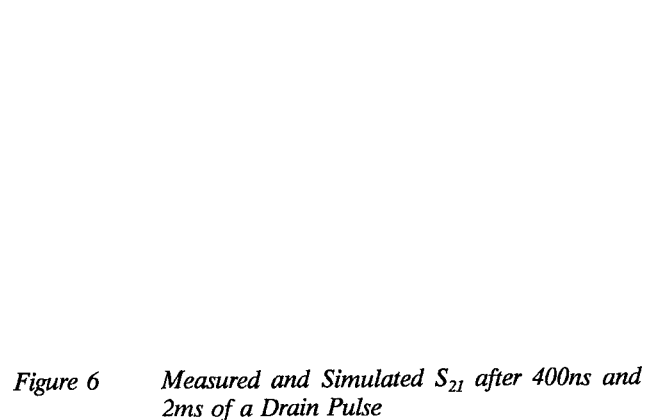*Figure 5*   *Gate-Source and Gate-Drain Capacitance as a Function of Temperature*

Figure 6   *Measured and Simulated S_{21} after 400ns and 2ms of a Drain Pulse*